ABSTRACT

Disclosed is a method for detecting electrical defects on test structures of a semiconductor die. The test structures includes a plurality of electrically-isolated test structures and a plurality of non-electrically-isolated test structures. The test structures each has a portion located partially within a scan area. The portion of the test structures located within the scan area is scanned to obtain voltage contrast images of the test structures' portions. In a multi-pixel processor, the obtained voltage contrast images are analyzed to determine whether there are defects present within the test structures. In a preferred embodiment, the multi-pixel processor operates with pixel resolution sizes in a range of about 25nm to 2000nm. In another aspect, the processor operates with a pixel size nominally equivalent to two times a width of the test structure's line width to maximize throughput at optimal signal to noise sensitivity. A computer readable medium having programming instructions for performing the above described methods is also disclosed.